In the Claims

1. (previously presented) An integrated circuit device comprising:

a dynamic random access memory (DRAM) cell having a storage capacitor formed within a deep trench in a substrate, the storage capacitor having an oxide trench collar, a gate conductor overlying said storage capacitor within said deep trench and a strap diffusion region adjacent the storage capacitor between the oxide trench collar and the gate conductor;

isolation regions on either side of the DRAM cell, the isolation regions extending below the gate conductor; and

a liner comprising a nitride compound adjacent the isolation regions and extending at least between each of the isolation regions and the gate conductor and to the oxide trench collar below the strap diffusion region.

2. (original) The integrated circuit device of claim 1 wherein the liner comprises a silicon-oxy-nitride compound.

3. (original) The integrated circuit device of claim 1 wherein the liner extends alongside and below the isolation regions.

4. (previously presented) An integrated circuit device comprising:

a dynamic random access memory (DRAM) cell having a storage capacitor formed within a deep trench in a substrate and a gate conductor overlying said storage capacitor within said deep trench, a region adjacent the gate conductor containing a dopant;

isolation regions on either side of the DRAM cell, the isolation regions extending below the gate conductor;

a liner comprising a nitride compound adjacent the isolation regions and extending at least between each of the isolation regions and the gate conductor; and

an oxide layer between the gate conductor and the dopant-containing region, and extending between the isolation regions,

wherein the oxide layer and isolation regions define corner regions of the gate conductor and dopant-containing region, and wherein the liner reduces dopant depletion in the corner regions during subsequent thermal processing of the DRAM cell.

5. (original) The integrated circuit device of claim 4 wherein the dopant-containing region adjacent the gate conductor comprises a channel.

6. (original) The integrated circuit device of claim 4 wherein the dopant comprises boron.

7. (previously presented) An integrated circuit device comprising:

a dynamic random access memory (DRAM) cell having a storage capacitor formed within a deep trench in a substrate and a gate conductor overlying said storage capacitor within said deep trench;

isolation regions on either side of the DRAM cell, the isolation regions extending below the gate conductor;

a liner comprising a nitride compound adjacent the isolation regions and extending at least between each of the isolation regions and the gate conductor; and

a planar support device adjacent the DRAM cell, the planar support device including a thermally produced oxidation layer.

8. (original) The integrated circuit device of claim 1 wherein the storage capacitor of the DRAM cell extends below the isolation regions and liner.

9. (original) The integrated circuit device of claim 1 wherein a vertical metal oxide semiconductor field effect transistor (MOSFET) comprising the gate conductor and a boron-doped channel overlies the storage capacitor.

10. (original) An integrated circuit device comprising:

a dynamic random access memory (DRAM) cell having a storage capacitor formed within a deep trench in a silicon substrate and a gate conductor overlying said storage capacitor within said deep trench, a region adjacent the gate conductor containing a boron dopant;

isolation regions on either side of the DRAM cell, the isolation regions extending below the gate conductor;

a liner comprising a silicon-oxy-nitride compound adjacent the isolation regions and extending at least between each of the isolation regions and the gate conductor; and

an oxide layer between the gate conductor and the boron dopant-containing region, and extending between the isolation regions, wherein the oxide layer and isolation regions define corner regions of the gate conductor and boron dopant-containing region, and wherein the liner reduces boron depletion in the corner regions during subsequent thermal processing of the DRAM cell.

11. (original) The integrated circuit device of claim 10 wherein the liner extends alongside and below the isolation regions.

12. (original) The integrated circuit device of claim 10 wherein the boron dopant-containing region adjacent the gate conductor comprises a channel, and wherein a vertical metal oxide semiconductor field effect transistor (MOSFET) comprising the gate conductor and the boron-doped channel overlies the storage capacitor.

13. (original) The integrated circuit device of claim 10 further including a planar support device adjacent the DRAM cell, the planar support device including a thermally produced oxidation layer.

14. (original) The integrated circuit device of claim 10 wherein the storage capacitor of the DRAM cell extends below the isolation regions and liner.

15-31. (cancelled)